REMARKS

Claims 1, 2, 4, 5, 7, 9, 21 and new claim 22 are pending in this application because Applicant elected Group I and Species V for prosecution in the response dated October 30, 2002 which included claims 1, 2, 4, 5, 7, 9 and 21. While the Examiner is examining claims 1 and 21, the applicants urge that claims 2, 4, 5, 7 and 9 still belong in Species V because Species V is not limited to FIG. 6A-D, but is actually covered in several drawings.

For example, the specification, page 29, lines 17-18, reads, "As shown in Fig. 6A, on an underlying structure 111 similar to that shown in Fig. 5A..." Further, page 27, lines 4-5 reads "For example, the underlying structure 111 is a structure that conductive plugs are embedded in the first lower insulating layer da1 shown in Fig. 4." The specification explains that FIGS. 4-6 are related and not necessarily exclusive species.

As a further example, a wiring layer comprising a barrier metal layer and a main wiring layer is repeatedly shown in Figures 1A-3I. In Fig. 1C, a barrier metal layer **15** and a main wiring layer **16** are shown. Similar wiring patterns are shown in Figs. 2A to 2G and 3A to 3I. Also, page 27, lines 25-26 reads, "As shown in Fig. 5B, a wiring layer 115 of a barrier metal layer and a main wiring layer is formed..." The wiring layer **115** in Fig. 6B should not be considered a separate species necessarily exclusive from that shown in earlier Figs., but rather Species V is shown in several drawings.

The claim amendments and new claim are supported as follows: Claim 1 (FIG. 6C) and Claim 22 (based on Claim 21).

FIGS. 12A-14B have been labeled with the term - RELATED ART - .

FIG. 1D has been amended to delete reference numbers 2 and 3.

The specification has been amended to reflect FIGS. 5A-6D.

The specification has been amended to correct minor informalities including those helpfully suggested by the Examiner.

Claims 1 and 21 stand rejected under 35 USC §102(e) as being anticipated by **Iguchi '363**. As now claimed, the applicant's invention is structurally different from and not anticipated by **Iguchi '363**.

As clearly shown in FIGS. 1 and 13-15 the polishing remains **21**, **22**, and **23** (col. 3. lines 52-53; col. 9, lines 9-10) are completely outside the Ta and insulation film layers. Polishing remains **21**, **22**, and **23** appear as residue in no particular pattern.

In contrast, Claim 1 as amended defines dummy wiring patterns defined in the interlevel wiring layer, i.e., damascene pattern embedded in the interlevel insulating film. Since the metal residue in **Iguchi '363** is located on the outer sidewall of the patterned insulating layer, it is not defined between a pair of sidewalls of the insulating layer and therefore not in a wiring pattern.

The FIGS of **Iguchi '363** clearly show that **Iguchi '363** is structurally different than the invention as now claimed.

With respect to claim 21, the office action states that **Iguchi '363** shows a first insulating

layer (2) having a lower dielectric constant than silicon oxide. **Iguchi '363** only describes "a silicon oxynitride film 2." Generally speaking, silicon nitride has a higher dielectric constant than silicon oxide, and silicon oxynitride has an intermediate dielectric constant between silicon nitride and silicon oxide. Since there is no special description, there is no reason to use special silicon oxynitride which has a lower dielectric constant than silicon oxide, in **Iguchi '363**. **Ishikawa '344** discloses silicon oxynitride which can have a lower dielectric constant than silicon oxide. **Ishikawa '344** teaches that the disclosed special silicon oxynitride layer has enhanced burying characteristics and water-permeability resistance and also has smaller dielectric constant and layer stress. The silicon oxynitride layer **2** in **Iguchi '363** appears to be used as an anti-oxidation layer for the underlying W plug, and also as an etching stopper layer for etching the insulating film **3.** There is no motivation to employ special silicon oxynitride in **Ishikawa '344**. As a result claim 21 is not anticipated by **Iguchi '363**.

It has been shown that **Iguchi '363** cannot logically anticipate the invention as now claimed because the polishing remains **Iguchi '363** are not conductor *patterns* in the peripheral area as claimed by the applicants.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number

indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/987,012

IN THE SPECIFICATION:

The paragraph beginning at line 22, page 5, has been rewritten as follows

Figs. 8A to [8D] 8C are cross sectional views showing a modification of the embodiment shown in Figs. 6A to 6D.

The paragraph beginning at line 5, page 10, has been rewritten as follows:

Referring to Fig. 12C, in order to avoid the influence of dishing, after the second insulating layer 18 is formed, its surface is planarized by CMP. It is difficult to perform CMP uniformly over the whole wafer surface. The wafer peripheral area is likely to be polished more than the wafer central area, because of a distribution of a pressure applied to the wafer, a distribution of a slurry supply amount and the like. There is, therefore, a tendency that the [first] second insulating layer 18 after CMP is thick in the wafer central area and thin in the wafer peripheral area.

The paragraph beginning at line 14, page 15, has been rewritten as follows:

Fig. 1D is a plane view of the wafer 1. In the effective wafer area indicated by hatched lines, hole patterns are formed, whereas in the peripheral wafer area around the effective wafer area, hole patterns are not formed. Since hole patterns are not formed in the peripheral wafer area, it is possible to prevent the second etching stopper layer 17 from being etched and the main wiring payer 16 from being oxidized and decomposed.

The paragraph beginning at line 16, page 21, has been rewritten as follows:

As shown in Fig. [13B] 3B, on the semiconductor wafer formed with wiring grooves and conductor grooves, a first barrier metal layer 15 and a first main wiring layer 16 are formed. For example, the barrier metal layer 15 is made of a Ta layer of 50 nm thick, and the main wiring layer 16 is made of a Cu layer of 1500 nm. Thereafter, CMP is performed to remove unnecessary regions of the main wiring layer 16 and barrier metal layer 15 on the surface of the silicon oxide layer 42.

The paragraph beginning at line 19, page 24, has been rewritten as follows:

On an active region defined by STI, an insulated gate electrode 5 and a side wall spacer 6 are formed, and on both sides of the gate electrode, source/drain regions S/D are formed through ion implantation. A first etching stopper layer s1 is formed covering the insulated gate electrode, and a first lower [insulting] insulating layer da1 is formed on the first etching stopper layer s1. A conductive plug is formed through the first lower insulating layer da1 and first etching stopper layer s1, the conductive plug being constituted on a barrier metal layer 7 and a wiring metal region 8.

The paragraph beginning at line 4, page 27, has been rewritten as follows:

As shown in Fig. 5A, on an underlying structure 111, an organic insulating film 112 made of, for example, SiLK, is coated to a thickness of 250nm. For example, the underlying structure 111 is a structure that conductive plugs are embedded in the first lower insulating layer da1 shown in Fig. 4. Conductive plugs 110 are not formed in the wafer edge area. Coated material in the peripheral wafer area is removed by rinsing using etchant by about 3mm +- 0.5mm from the wafer edge. Next,

an insulating film 113 made of, for example, a silicon oxide film of about 250 nm thick, is deposited by CVD to cover the whole surface of the organic insulating layer 112.

The paragraph beginning at line 13, page 39, has been rewritten as follows:

As shown in Fig. 9L, the wiring layer 25 is polished by CMP from its surface to remove unnecessary regions of the wiring layer 25 and metal layer 47. In this case, in the wafer edge area, polishing is stopped in the state that the wiring layer 25 covers the side wall of the organic insulating layer 45. An etching stopper layer 26 made of, for example, an SiN layer of 50 nm thick or a surface protective layer is formed covering the surface of the wiring layer 25.

IN THE CLAIMS:

Please amend Claim 1, as follows:

1. (Amended) A semiconductor wafer device comprising:

a semiconductor wafer having a circuit area disposed in a central area of said semiconductor wafer and a peripheral area of said semiconductor wafer not formed with circuits;

a number of semiconductor elements formed in the circuit area;

a multi-layer wiring structure formed in the circuit area and having multi-layer wirings connected to said semiconductor elements and interlevel insulating films, at least some of the multi-layer wirings being damascene wirings including wiring patterns and via conductors embedded in the interlevel insulating films; and

a multi-layer structure formed in the peripheral area, having insulating films made of a same

materials as the interlevel insulating films and conductor patterns, defined between sidewalls of said insulating films, made of same materials as the wiring patterns and not having conductor patterns corresponding to the via conductors.